

- Verilog code :

```
module Lcd_Display (clk, lcd_rs, lcd_rw, lcd_e, lcd_4, lcd_5, lcd_6,  
lcd_7);  
parameter n = 27;  
parameter k = 17;  
(* LOC="E12" *) input clk; // synthesis attribute PERIOD clk "100.0 MHz"  
reg [n-1:0] count=0;  
reg lcd_busy=1;  
reg lcd_stb;  
reg [5:0] lcd_code;  
reg [6:0] lcd_stuff;  
(* LOC="Y14" *) output reg lcd_rs;  
(* LOC="W13" *) output reg lcd_rw;  
(* LOC="Y15" *) output reg lcd_7;  
(* LOC="AB16" *) output reg lcd_6;  
(* LOC="Y16" *) output reg lcd_5;
```

# Lcd Display Using Verilog Code

**Patrick Vollmar**



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