

General notes

Energy stored in an inductor

$E = \frac{1}{2} L I^2$

- remember voltage stored in series, current stored in branches

OP-AMP

- Gain equation

$G(\omega) = \frac{V_o}{V_i}$



$V_i R_2 + V_o R_1 = 0$
 $V_o = -\frac{R_2}{R_1} V_i$

$V_o = -\frac{R_2}{R_1} V_i$
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- when $R_1 = R_2$ gain is -1
- when $R_2 > R_1$ gain is $-R_2/R_1$

- Closing loop ideal output voltage is an open circuit the present output voltage (from the supply rails) this results in the output being buffered which can distort the signal and introduce hum/noise



- Bandwidth
- Calculate max gain without for opening and bandwidth
- Gain: 1000
- $1000 = \frac{V_o}{V_i}$
- $V_o = 1000 V_i$
- $V_i = \frac{V_o}{1000}$
- $V_i = \frac{10V}{1000} = 10mV$
- $V_o = 10V$
- $V_i = 10mV$
- $V_o = 10V$

Mesh analysis KVL

Σ V around loop



$i_1 = i_2$
 $V_s - i_1 R_1 - i_1 R_2 - V_o = 0$
 $V_s - i_1 (R_1 + R_2) - V_o = 0$
 $V_s - i_1 (R_1 + R_2) - V_o = 0$
 $V_s - i_1 (R_1 + R_2) - V_o = 0$

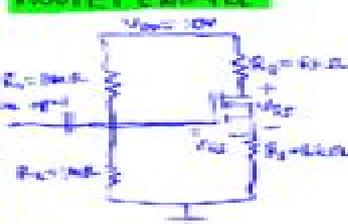
Thevenin voltage OC load
 Norton current SC load
 Current divider

$I_o = \frac{R_2}{R_1 + R_2} I_N$
 $V_s = \frac{R_2}{R_1 + R_2} V_{th}$

Node analysis (KCL)

$\sum i_{in} = \sum i_{out}$

NOSFET EXAMPLE



• Gate voltage V_G
 $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$
 $V_G = 5V$

- expression for gate source voltage V_{GS} in terms of gate voltage current and drain current I_D

• KVL around gate loop
 $V_G - V_{GS} - I_D R_S = 0$
 $V_{GS} = 5 - 1000 I_D$

• MOSFET bias in Sat region determine drain current I_D
 $I_D = K(V_{GS} - V_{GS(th)})^2$
 $I_D = K(5 - 1000 I_D - 2)^2$

$I_D = 0.5 \times 10^{-4} (5 - 1000 I_D - 2)^2$
 $I_D = 0.5 \times 10^{-4} (3 - 1000 I_D)^2$
 $I_D = 0.5 \times 10^{-4} (9 - 6000 I_D + 1000000 I_D^2)$
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Instrumental amplifiers

- used when we want to amplify the difference between two signals. This allows us to cancel out common mode noise. An example would be in an ECG or Wheatstone bridge

Temperature detector



Explain this op amp

- making follow
- adds input at one part of load for another, partly a body of water used and by the region

- Determine 2 values for gate source voltage V_{GS} and drain current I_D in the Sat region
 $V_{GS} = 5 - 1000 I_D$
 $I_D = 0.5 \times 10^{-4} (5 - 1000 I_D - 2)^2$
 $I_D = 0.5 \times 10^{-4} (3 - 1000 I_D)^2$
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Diode Determine if diode state is conducting



- with only conduct is forward biased, if $V_o > 0$ then FS
- assume worst possible for analysis and SC
- both analysis with $V_o = 10 - 2i_1 = 0$ but SC with $V_o = 15 - 5i_2 = 0$ but SC $V_o < 0$ so were wrong and not conducting

Impedance

$Z_{in} = Z_1 + Z_2 + Z_3$

Inductor

- $V_L = L \frac{di}{dt}$ voltage across inductor inductor = 0



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Daniel F McAuley



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